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# Increasing the accuracy of an analogue-to-digital converter (ADC) with an intermediate voltage-to-frequency conversion

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The article proposes an approach to increasing the resolution of integrated analogue-to-digital (ADC) converters with intermediate voltage-to-frequency conversion (VFC). At sampling rate1 kHz was achieved effective number of bits (ENOB) from 12 to 16. In addition, an approach to compensating for the non-linearity of voltage-to-frequency conversion was proposed. Across the range of measured voltages from 100 mV to 8 V, the voltage measurement error comprised no more than ±0.025 %, which corresponds to a five-and-a-half-bit voltmeter. The proposed device was implemented exclusively on mass-produced chips. The six independent ADC channels, implemented on 1316PP1AU VFCs, are serviced by a single 1986VE91 microcontroller, with the processor loading with the task of improving accuracy being no more than 10 %.

*Keywords*: analog-to-digital converter, sigma delta, resolution, voltage-to-frequency conversion

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## Introduction, relevance of the problem

The accuracy of electromechanical instruments depends on the accuracy of primary sensors and electrical measurements. As the sensing accuracy is constantly improved, this requires better accuracy of electrical measurements.

Now, the best practices for acquiring highly accurate digitized sensing data normally involve sigma-delta analog-to-digital converters (ADC) with high resolution. Unfortunately, Russia faces difficulties in terms of large-scale production of highly accurate sigma-delta ADCs. Along with that, there is an option to use the ADC based on intermediate voltage-to-frequency conversion (VFC). For example, the 1316PP1AU chip [1, 2] is the workhorse used in commercial products manufactured in Russia [1, 2]. This chip has some major drawbacks:

– low resolution;

– dead zone in the zero junction area.

A. A. Zakharov conducted an in-depth analysis of the influence of the dead zone on the performance of gyroscopic instruments [3].

According to the latest modern tendencies, the applied sensors are becoming smarter thanks to embedded microcontrollers that allow to enhance functional capabilities and introduce error compensation, self-test functions, etc. At the same time, the applicable microcontoller serves to improve VFC by enhancing resolution, enabling calibration and compensating the inherited non-linearity.

The first part of the paper proposes a method that allows to simultaneously enhance resolution of the VFC chip and eliminate the dead zone. The method is patented (utility patent RU2731168).

The second part of the paper proposes a VFC calibration method with compensation of the S-shaped dependence of measurement error on input voltage.

## Enhancement of VFC-nonius-based ADC resolution

The functional diagram of the device is shown in Figure 1.

To understand the essence of the proposed method, firstly, we will analyse operation of the VFC-based ADC using the 1316PP1AU chip as an example [2] without resolution enhancement.

The input voltage is constantly integrated. The integrator output voltage is compared with reference levels. When the integrator voltage exceeds level Uth+, the output count pulse and integrator reset pulse will be generated. When the integrator output voltage drops below level Uth-, the second similar pulses are generated. While the reset pulse is being active, the integrator input receives a highly stable current, the polarity of which corresponds to the opposite polarity of the input signal. The number of output reset pulses of both positive and negative polarity is counted by the up/down pulse counter.

The counter's output code is read out as per the external "Sample" pulse, and then the counter is reset.

Therefore, the conversion scale coefficient is determined by reference voltages and by the ratio of integrator input resistor resistance to the integrator reset circuit resistor resistance.

Deficiencies of this engineering solution are low resolution and the presence of the dead zone in the zero junction area.

Below we will give a numerical example. For VFC chips, the higher the clock speed, the lower the accuracy. In particular, for the 1316PP1AU chip, the output frequency at a grounded input is 3 kHz at fc = 8 MHz, K = 20 Hz/mV and, therefore, the bias voltage reduced to the input is 150 μV. At fc = 4 MHz, K = 10 Hz/mV, respectively, the output frequency is 0.5 Hz, and the bias voltage reduced to the input is 50 μV. Thus, it is reasonable to select K = 10 Hz/mV to achieve the maximum accuracy. Therefore, at sampling rate of once per

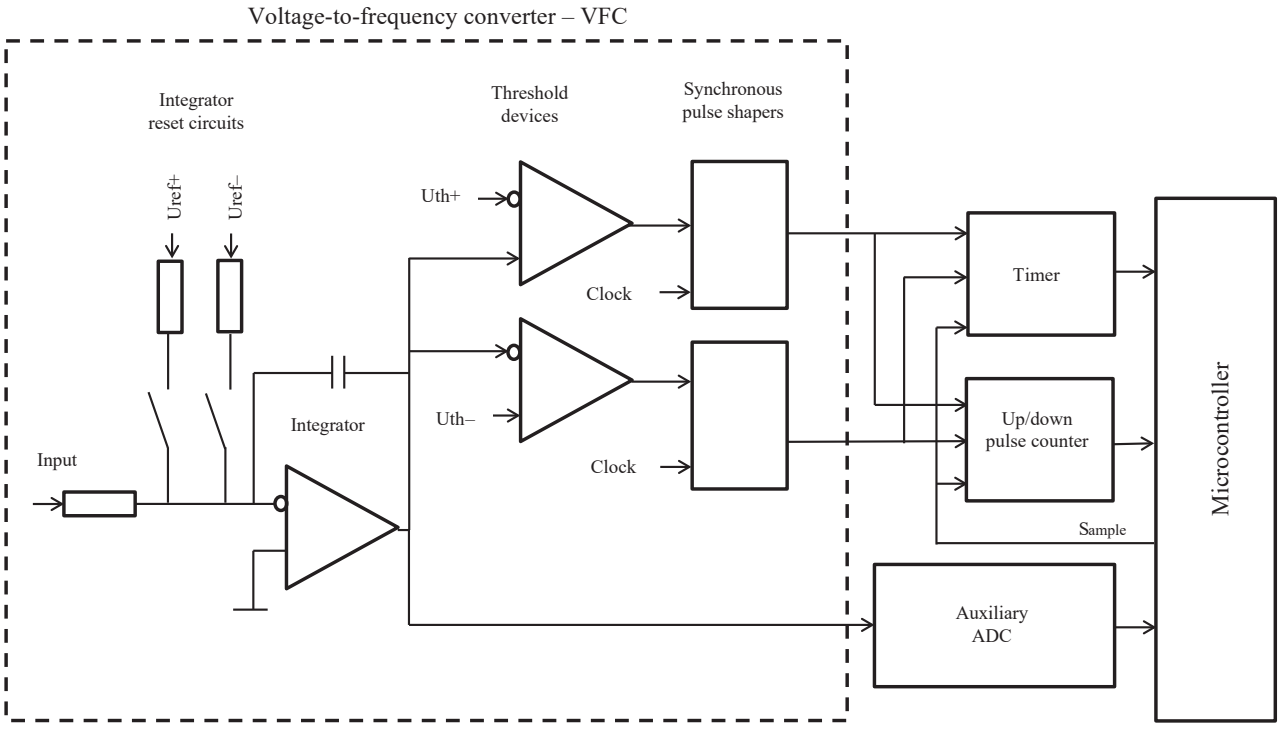


**Fig. 1.** Functional diagram of the device

millisecond, the weight of a single count pulse is equal to 100 mV or more than one percent of the maximum value being measured.

There is a well-known method of resolution enhancement, digitizing of output voltages of the integrator included in the VFC during pulse readout by an auxiliary ADC. Based on the difference between voltages at the beginning and at the end of the sampling period, we can calculate fractions of count pulses [4, 5, 9].

Figure 2 shows oscillograms of VFC integrator output voltage. If there is no count pulse for the time period between two readout pulses, but the integrator output voltage has changed, the input voltage is determined by a change in the integrator output voltage. Also, the converter resolution is increased with account for the difference between voltages at the beginning and at the and of the measurement interval.

The exact value of the count pulse repetition frequency is calculated by formula:

$$F = \frac{Q_n + \frac{U_i - U_{i-1}}{U_h}}{T}, \quad (1)$$

where $Q_n$ – number of count pulses or number of integrator reset cycles for time period T.

But this method also has its drawback. If the "Sample" count pulse coincides with the integrator reset pulse time, the voltage recorded by an auxiliary ADC will not correspond to the value shown in Figure 2, and hence we will obtain an erroneous result. Voltage oscillograms for the described case are shown in Figures 3 and 4.

To eliminate the drawback, we measure the time of arrival of count pulses Δt. If the readout pulse takes place during the time period of integrator reset and if the count pulse has been counted, we will consider Figure 3.

To obtain the correct result of calculation by formula (1), we substitute the readings of an auxiliary ADC with value $U_a$ calculated by formula (2):

$$U_a = U_{th} + U_h - \frac{U_h Q_n \Delta t}{T}. \quad (2)$$

If the count pulse is not counted, we will consider Figure 4.

Similarly, we substitute the readings of an auxiliary ADC with value Ua1 calculated by formula (3):

$$U_{a1} = U_{th} - \frac{U_h Q_n \Delta t}{T}. \quad (3)$$

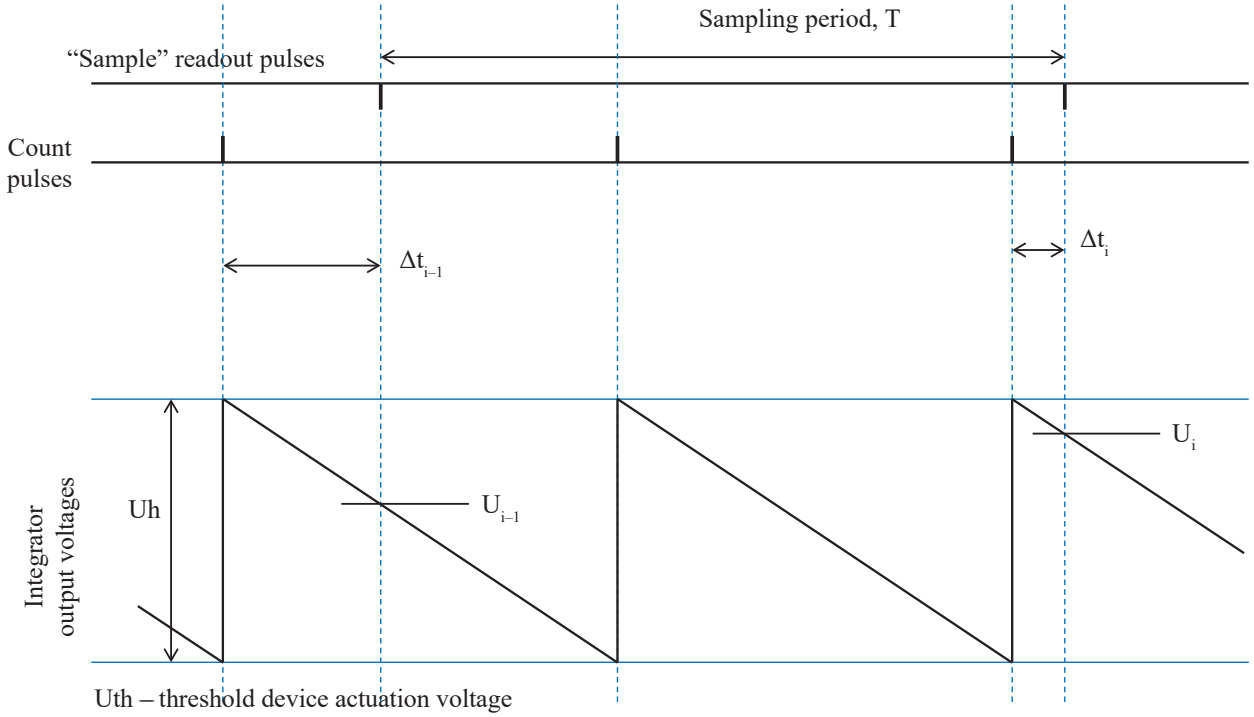


**Fig. 2.** VFC integrator output voltage oscillograms

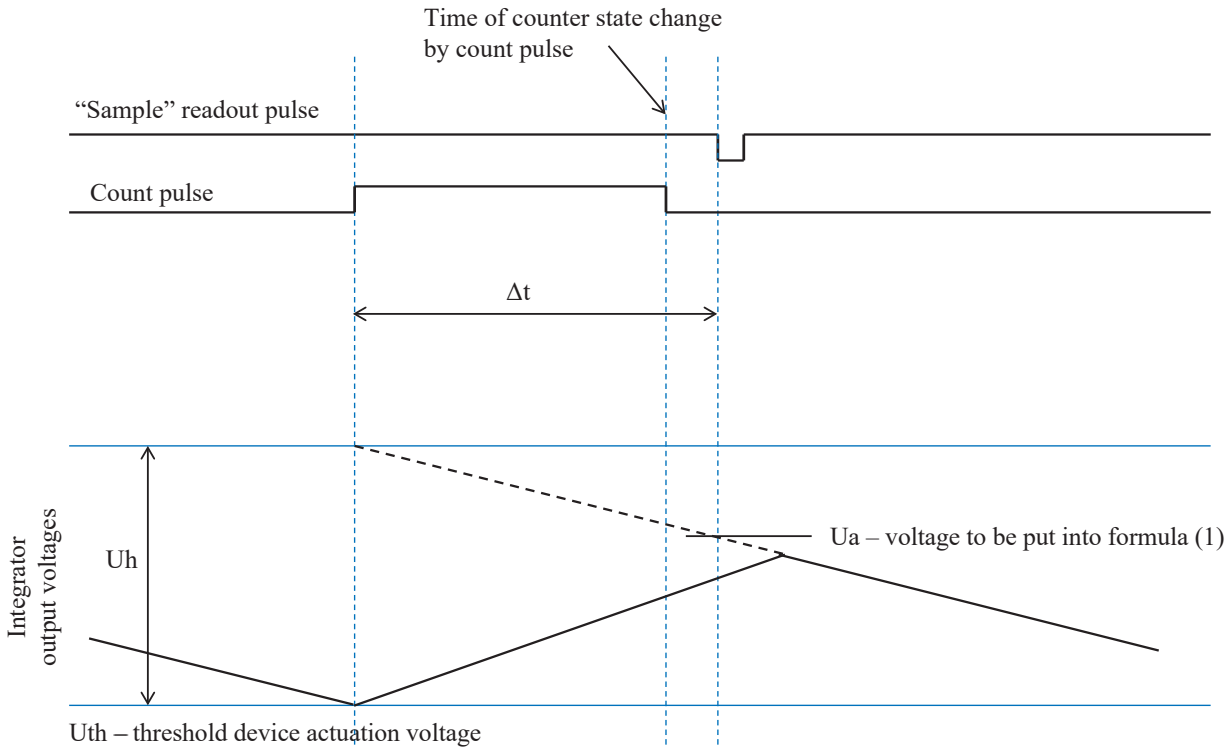


**Fig. 3.** VFC integrator output voltage oscillograms with the readout pulse coinciding with the integrator reset time and with the count pulse counted before arrival of readout pulse

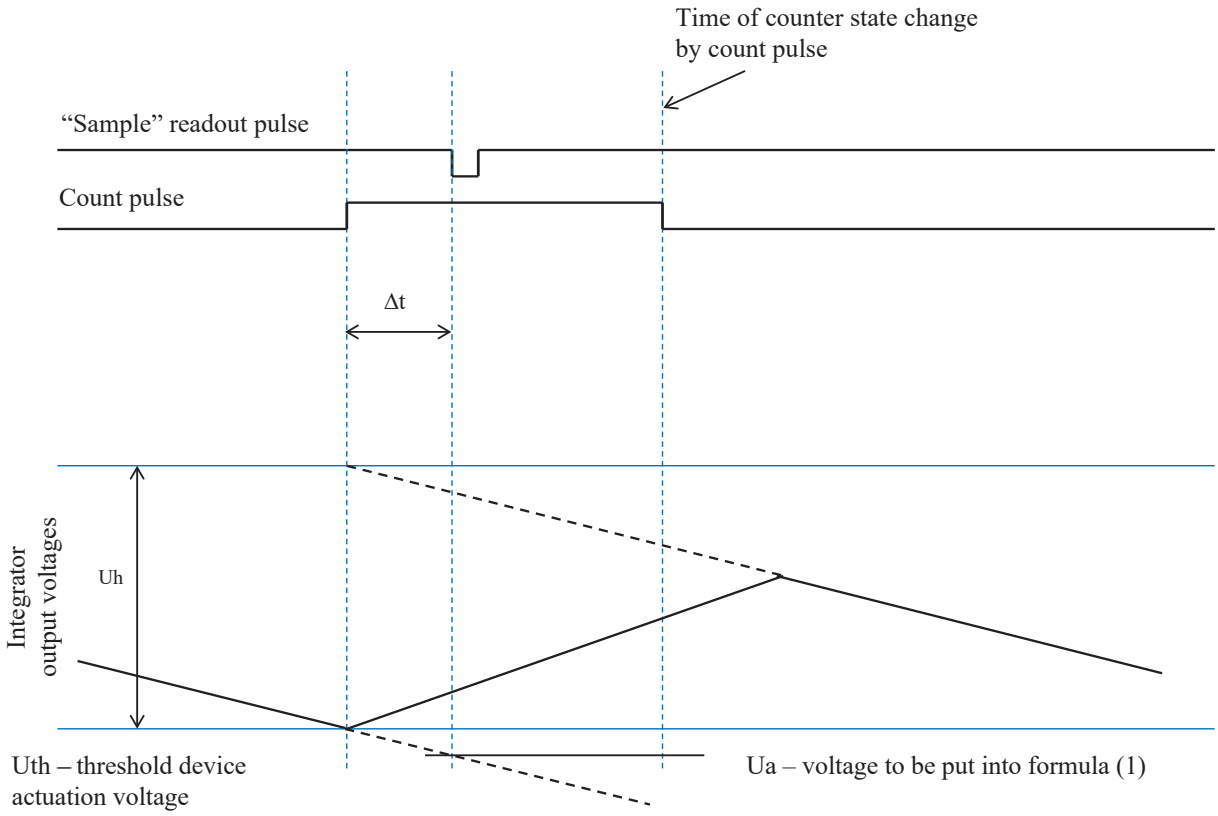


**Fig. 4.** VFC integrator output voltage oscillograms with the readout pulse coinciding with the integrator reset time and with the count pulse not counted before arrival of readout pulse

The proposed engineering solution was patented (utility patent No. U2731168.).

We developed a printed circuit board, where single microcontroller 1986VE91 was connected to 6 converters 1316PP1AU. It takes minimum complications of the hardware design and consists only in matching the integrator output voltage range of ±5 V and auxiliary ADC input range of 0 to 3 V. The microcontroller has an integrated software, which executes the algorithm for resolution enhancement. At interrogation frequency of once per 1 ms, the program execution time is less than 10 % of the processor time. Thus, the microcontroller has the remaining computational resources available for other purposes.

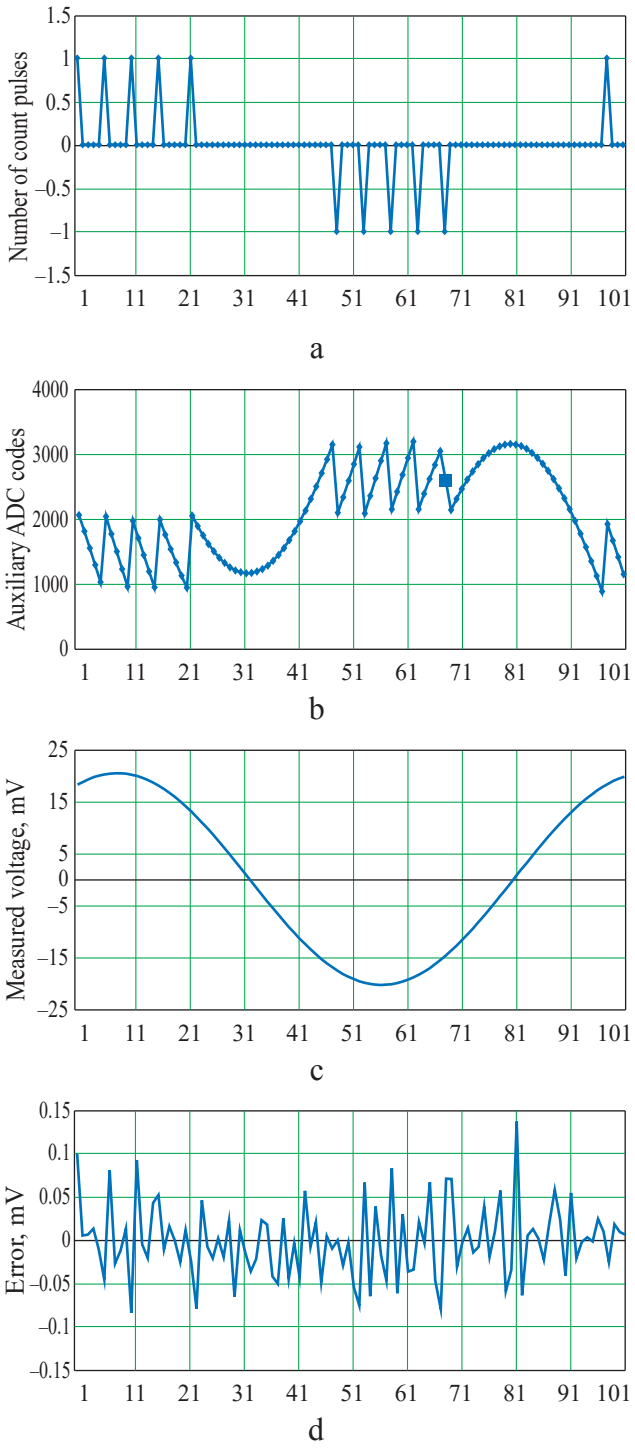


**Fig. 5.** Operation at sinusoidal signal of 20 mV, 10 Hz: a – number of count pulses, b – auxiliary ADC codes, c – measured voltage, mV, d – error, mV

To illustrate the proposed method, the following experiment was carried out. The 1316PP1AU converter input receives a sinusoidal signal of amplitude of 20 mV and frequency of 10 Hz. Converter readings were taken at the intervals of 1.024 ms and recorded to the file. Figure 5 shows a fragment of the results for 100 readings.

Figure 5a represents the number of count pulses per reading. This corresponds to the operation mode without nonius resolution enhancement. According to Figure 5a, all the data indicating the actual shape of the input signal are lost and there is a large dead zone near the zero junction area.

Figure 5b shows the output voltage of the integrator included in the 1316PP1AU converter. The voltage was digitized with the help of an auxiliary ADC included in the 1986VE91 microcontroller.

With the input signal of positive polarity, the integrator output voltage gradually decreases at a rate proportional to the input voltage. Once the threshold voltage is reached, the integrator will be reset with simultaneous generation of a count pulse. In the input voltage zero junction area, the rate of change of integrator voltage decreases and changes its sign after the polarity of input voltage changes. After the second threshold voltage is reached, the integrator will be reset again, and count pulses of the other polarity will be generated, respectively.

Special attention shall be paid to the reading indicated with a large square marker in Figure 5b.

At that moment, auxiliary ADC measurement took place during integrator reset.

Figure 5c shows the result of voltage measurement algorithm. It is obvious that the shape of the input sinusoidal signal is restored. It is necessary to emphasize that when the interrogation coincided with integrator reset, the algorithm substituted the reading of the auxiliary ADC with the information on the time of arrival of a count pulse and, as a result, there was no failure.

To estimate the noise level, the output signal was approximated by the ideal sinusoidal signal using the least squares method. The ideal signal was subtracted from the measured one. The signal difference is shown in Figure 5d. It is obvious that the error is substantially smaller than one millivolt. The standard deviation of the error, shown in Figure 5d is 50 μV. This value corresponds to the effective number of bits (ENOB) equal to 16.

Also, to estimate noise characteristics, the results at constant input voltage were recorded. Figure 6 shows a zero signal when the input is short-circuited. Figure 7 shows a signal at constant voltage of 8 V.

According to comparison of Figure 7 with Figure 6 and 5d, high values of input voltage lead to an increase of the absolute values of the variable component.

In order to explain this peculiarity, we will analyse the causes of noise generation in different operation modes.

When the input voltage is low, in most cases, the result can be found based on readings of an auxiliary ADC. On rare occasions, when the readout pulse coincides with the integrator reset time, the member depending on Δt in formulae (2) and (3) is small. Therefore, measurement discreteness Δt makes a minor contribution to the total noise level.

If the input voltage is high, the frequency being measured and the probability of coincidence of the readout pulse with the integrator reset time are high as well. Thus, in most cases, formulae (2) and (3) will apply, and, therefore, measurement discreetness Δt will make a major contribution to measurement noise. In the 1316PP1AU chip, the time of count pulse generation is bound to clock speed of 4 MHz.

For example, at measured voltage of 8 V and pulse frequency of 80 kHz, measurement error Δt equal to 250 ns will result in frequency measurement error of 20 Hz.

These calculation are proven by the results shown in Figure 7. The resulted mean square deviation is 1 mV and the relevant equivalent number of bits is 12.

The noise error registered during execution of the proposed algorithm has a distinguishing statistical characteristic. If the measurement time is N times higher, the voltage measurement error is N times lower as well. This statistical evidence was checked in the range of 1, 2, 4, and 8 ms and maintained within a time period of around one second.

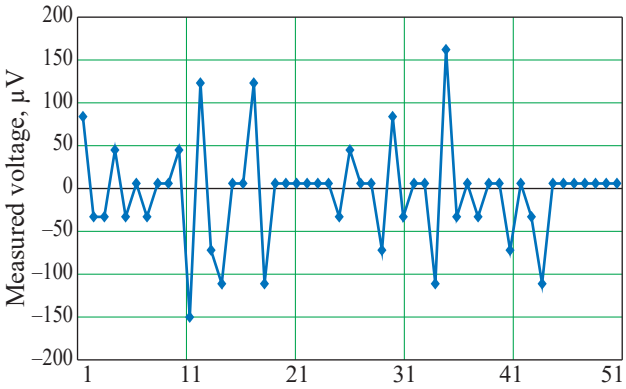


**Fig. 6.** Zero signal when the input is short-circuited

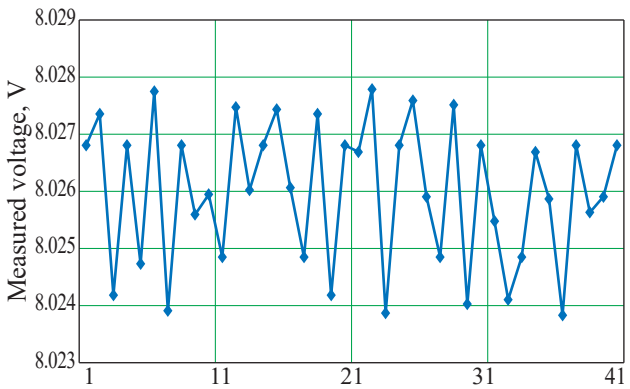


**Fig. 7.** Signal at constant voltage of 8 V

**Temperature stability of nonius compensation**

A variation of the integrator's time constant makes a major contribution to the instability of calibration constant Uh. The time constant is equal to the capacitor capacity multiplied by the resistor resistance.

Typical TCR of internal resistors of the 1316PP1AU chip is 500 ppm. Instability is not more than 100 ppm. To ensure maximum stability, we exclude warm-up drifts of the integrator's internal capacitor and use an external ceramic capacitor that belongs to temperature stability group MP0.

Without temperature compensation, a temperature deviation from normal conditions to minus 60 °C will cause additional noise equal to 4 % of 100 mV, or 4 mV. If such a level of extra noise is not acceptable, it is allowed to carry out additional temperature calibration Uh and minimize the noise level.

**Comparison of the obtained result with Russian and foreign equivalents**

Comparison of the effective number of bits for chip made in Russia and abroad at sampling rate of 1 kHz is given in the table below.

Let us describe the chips made in the Russian Federation.

Unfortunately, multi-channel VFC chips 1316NKh035 [7] and 5400TR065-012 [8] being newly developed are not compatible with the "nonius" resolution enhancement, because the required signals are not routed out of the chips.

The first row of the comparison data table contains the effective number of bits for the 1316PP1AU chip without "nonius" application.

The second row contains data of three-channel VFC chip 5400TR065-012, its parameters corresponding to parameters of 1316PP1AU.

For the 1316NKh035 chip, as well as for 1316PP1AU, an increase in the clock speed leads to lower accuracy. That is why, in order to ensure maximum accuracy, it is reasonable to select the minimum frequency – fc = 8 MHz and, therefore, the conversion coefficient of 50 kHz/V. Therefore, at sampling rate of 1 kHz, the weight of a single pulse will be 20 mV. During experiment, the results of which are shown in Figure 5, we selected a signal amplitude of 20 mV for comparison.

Design specifications for the 1273PV1R, 1273PVR, 1273PV9R chips, unlike their foreign-made equivalent AD7710, do not stipulate bias voltages. This makes them difficult to use for measuring constant voltage. Moreover, it takes much time to deliver these chips to customers.

At the time of writing this paper, the works related to the 24-bit sigma-delta ADC MLDR 116 project were interrupted. Preliminary data on MLDR 116 is given for reference.

Comparison with the table data proves that the obtained result is better than those demonstrated by chips made in the Russian Federation and is close to the world-class products.

Table

Comparison of the effective number of bits, Russian chips vs. foreign-made chips

| Country | Manufacturer | Technology | Chip type | Effective number of bits |
|---|---|---|---|---|
| Russian Federation | Milandr | VFC | 1316PP1AU | 7.3 |
| | DTs "Soyuz" | VFC | 5400TR065-012 | 7.3 |
| | Milandr | VFC | 1316NKh035 | 8.6 |
| | NPO "SKTB ES" | 24-bit sigma-delta ADC | 1273PV1R, 1273PV8R, 1273PV9R | 10.5 |
| | Milandr | 24-bit sigma-delta ADC | MLDR116 | 15.9 |
| USA | Analog Devices | 24-bit sigma-delta ADC | AD7710 | 10.5 |
| | Texas Instruments | 24-bit sigma-delta ADC | ADS1248 | 17.2 |
| | Texas Instruments | 31-bit sigma-delta ADC | ADS1283 | 20 |

## Elimination of non-linearity

After resolution enhancement is implemented, it becomes possible to conduct accurate measurements for a short time period, for instance, within one second. Therefore, more accurate calibration of the converter as a voltage meter becomes an urgent problem.

The integrating converter has a non-linear S-shaped dependence of measurement error on the input voltage.

The S-shaped curve is basically caused by the dependence of integrator amplifier Ku on the input voltage, plus variable dynamic characteristics of the amplifier.

We have found out that the curve can be satisfactorily approximated by polynomials of the 2nd degree.

During calibration, voltages in the range of 0.25; 0.5; 1…8 V were successively fed to the circuit board input. Results were averaged in each mode within 1 second, and then, using the least squares method, coefficients of the polynomial of the 2nd degree, expressed in percent, were determined as per the criterion of relative error minimization.

Calibration was repeated for both positive and negative polarity of input voltage. As a result, an individual set of coefficients was obtained for each polarity.

Results of voltage measurements for six channels are shown in Figure 8a. It is evident that the voltage measurement error lies within ±0.025 %.

Comparison of results of calibration by polynomials of the 1st and 2nd degree is shown in Figure 8b. Errors during calibration by polynomials of the 1st degree have a typical S-shaped form and reach the value equal to several millivolts. As a result of calibration by a polynomial of the 2nd degree, only random irregular errors remain.

## Conclusions

The paper proposes a method that allows to enhance the resolution of integrating ADC converters with intermediate voltage-to-frequency conversion (VFC). Application of the proposed method allows to achieve a higher resolution in comparison to all chips mass-produced in the Russian Federation and is comparable with the world-class products. At sampling time of 1 ms, the effective number of bits (ENOB) is increased from 7.3 to 12–16. By comparison, the best Russian precision ADCs provide ENOB of 10.5.

Also, the paper proposes an DC calibration method, using polynomials of the 2nd degree with attainable accuracy of voltage measurement within ±0.025 %.

This device can be implemented using mass-produced chips. This takes minimum complications of hardware design (few resistors are to be added, plus several additional tracks on the printed circuit board).

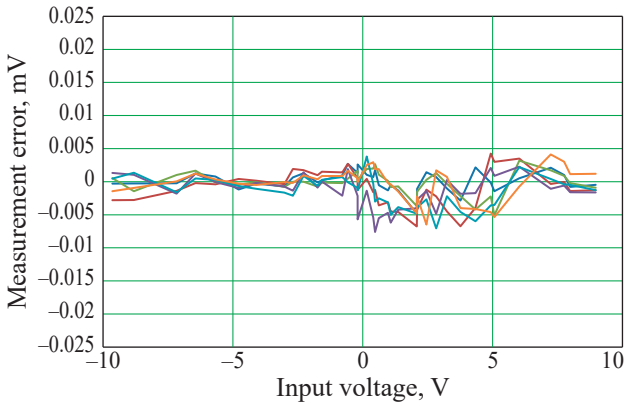


**Fig. 8a.** Dependence of relative measurement error on input voltage

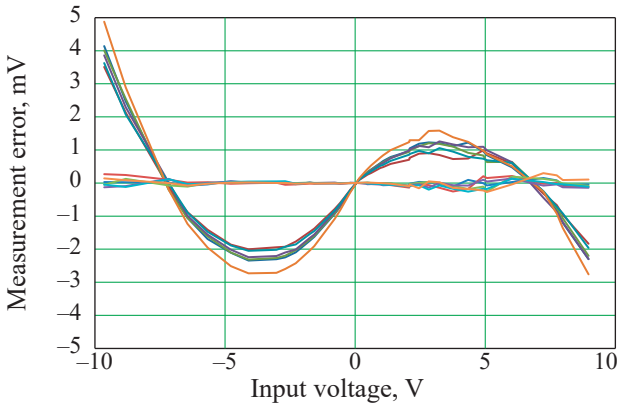


**Fig. 8b.** Comparison of absolute measurement errors during calibration by polynomials of the 1st and 2nd order

Moreover, the proposed method can be applied to newly developed multi-channel ADC chips.

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# Повышение точности АЦП с промежуточным преобразованием в частоту

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В статье предложен способ повышения разрешающей способности интегрирующих аналого-цифровых преобразователей (АЦП) с промежуточным преобразованием в частоту (ПНЧ). При частоте дискретизации 1 кГц достигнуто эффективное число разрядов АЦП (ENOB) от 12 до 16. Также предложен способ компенсации нелинейности преобразования напряжения в частоту. В диапазоне измеряемых напряжений от 100 мВ до 8 В достигнута погрешность измерения напряжения не более ±0,025 %, что соответствует пяти с половиной разрядному вольтметру. Предлагаемое устройство реализовано исключительно на серийно выпускаемых микросхемах. Шесть независимых каналов АЦП, реализованных на микросхемах ПНЧ 1316ПП1АУ, обслуживаются одним микроконтроллером 1986ВЕ91, при этом загрузка процессора поставленной задачей повышения точности составляет не более 10 %.

*Ключевые слова:* аналого-цифровой преобразователь, сигма-дельта, разрешающая способность, преобразование напряжения в частоту.

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Область научных интересов: электромеханические приборы и преобразования.